



For Immediate Release

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**CIRANOVA RELEASES INDUSTRY'S FIRST AUTOMATED ANALOG LAYOUT SOLUTION
DELIVERING PRODUCTION-QUALITY RESULTS**

**Ciranova Helix™ Produces High Quality, Design-Rule-Correct Placement in Minutes;
Dramatically Shortens Time to Market and Enables Analog IP Migration**

SANTA CLARA, Calif. – June 2, 2008 – Ciranova™, Inc. today unveiled Ciranova Helix, the industry's first automated analog layout solution that optimizes both circuit and device layout simultaneously, delivering design-rule-correct placement comparable in quality to that produced by an experienced layout designer. Using Ciranova Helix, analog and custom designers can explore multiple layout alternatives in minutes, allowing them to get higher-quality designs to market in a fraction of the time needed by conventional methods.

For an analog layout automation tool to deliver production-ready results, it must simultaneously optimize circuit design requirements (matching, symmetry) with device layout requirements (device and contact ring abutment, well merging), while always obeying process requirements (design and DFM rules). Previous attempts at analog layout automation failed to gain wide acceptance because they compromised one or more of these three requirements. Ciranova Helix is the first general-purpose analog layout automation tool to achieve all three.

Ciranova Helix' primary inputs are a SPICE netlist and a Process Design Kit (PDK) containing either Cadence SKILL PCells or Ciranova PyCells™, such as those in the Interoperable PCell Library (www.iplnow.com). Designers may also specify symmetry, device matching, and other high-level circuit intent, which is obeyed by the tool no matter which PCells and process technology are used; this facilitates rapid analog IP migration. The output is full device-level placement, DRC-correct, in either OpenAccess or GDS format. Helix is a native OpenAccess tool

that integrates seamlessly with OpenAccess-compatible layout editors such as Cadence Virtuoso, Springsoft Laker and Magma Titan, as well as DRC tools such as Mentor Graphics Calibre and Synopsys Hercules.

“Analog and mixed-signal design is the last major EDA market not served by automated layout methods,” said Eric Filseth, Ciranova CEO. “Up to now, the tools simply haven’t delivered results acceptable to analog engineers, and in a timeframe of relevance. But with analog and mixed-signal content now a major bottleneck in SoC design, there’s pent-up demand for automation. Helix builds on our proven PyCell technology to enable large and practical productivity gains at the full-circuit level.”

Availability

Ciranova Helix is available now. Foundry processes from 250nm to 40nm are currently supported with more under development. Ciranova Helix is currently supported on 32-bit and 64-bit Linux, Solaris 8 and Solaris 10 and Microsoft Windows. For pricing information, contact Ciranova.

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