



**For Immediate Release**

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**CIRANOVA HELIX PROVIDES 28nm SUPPORT FOR  
TSMC ANALOG MIXED-SIGNAL REFERENCE FLOW 2.0**

June 3, 2011, Santa Clara California. Ciranova® Inc., a technology leader in analog IC physical design automation, announced today that its Ciranova Helix® custom IC layout automation software has been selected for LDE-Aware Automatic Placement in TSMC Analog Mixed-Signal Reference Flow 2.0, one of the critical components of TSMC 28nm design infrastructure.

“We have worked closely with Ciranova to incorporate the benefits of their technology in the TSMC Analog Mixed Signal Reference Flow 2.0 and the TSMC iPDK,” said Suk Lee, director of Design Infrastructure Marketing at TSMC. “We have demonstrated that Ciranova Helix can support our layout dependent effects (LDE) solutions, enabling significant improvement in custom design productivity at 28nm.”

Helix directly supports TSMC's LDE API for LDE-aware automatic placement to quickly create multiple layout choices that are LDE aware and DRC correct, in a fraction of the time required for manual layout.

At 28nm, SoC design has become so complex that timely success requires collaboration by many parties: foundries, IP suppliers, EDA companies, design service providers and others; hence interoperability is of critical importance. Helix supports industry standards like OpenAccess and iPDKs that promote industry collaboration and interoperability.

“Customers tell us that layout is getting more challenging at 28nm,” said Eric Filseth, president and CEO of Ciranova. “Design rule complexity is driving adoption of much more automated

methods, and TSMC is leading ecosystem partners with its Analog Mixed Signal Reference Flow 2.0. TSMC's customers at 28nm will see big time-to-market benefits.”

### **About Ciranova**

Ciranova is an electronic design automation (EDA) company focused on large productivity improvements in RF, analog and mixed-signal IC physical design. Complementary to existing design flows, Ciranova technology dramatically reduces the time and effort needed to develop device-level layout at both the circuit and PDK levels. Ciranova is a founding member of the Interoperable PDK Libraries (IPL) Alliance and supports the Si2 OpenAccess database. For more information please visit <http://www.ciranova.com>.

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