



For Immediate Release

For more information, contact:

Dave Millman
Ciranova, Inc.
+1 408 553-6083
dave@ciranova.com

**CIRANOVA HELIX SELECTED IN
TSMC ANALOG MIXED-SIGNAL REFERENCE FLOW 1.0
FOR PHYSICAL DESIGN AUTOMATION**

June 9, 2010, Santa Clara California. Ciranova, Inc., a leader in automated physical design for analog and mixed-signal ICs, announced today that its Ciranova Helix® custom IC layout automation software has been included in TSMC's OpenAccess-based Analog/Mixed-Signal (AMS) Reference Flow 1.0 targeting TSMC 28nm advanced process technology.

Helix was used within the TSMC flow to floorplan and place a reference phase-locked loop (PLL) design. The transistor-level placement passed all of its target combination of minimum, recommended, and custom process design rules, including many DFM-related rules such as conditionals, fill densities and grids. In the flow, the Helix placement was then routed using software from Pyxis Technology, Inc.

The PLL design contains approximately 10,000 devices; Helix run times were about ten minutes on a 4-CPU machine.

"We were pleased with Helix' ability to generate high quality and DRC-correct layout in an automated flow," said Tom Quan, deputy director of design methodology and service marketing at TSMC.

Ciranova Helix is a plug-and-play solution that works in any OpenAccess-based design flow to accelerate and improve predictability in custom IC layout; it works with a variety of libraries including parameterized cells (PCells), TSMC Analog Base Cells™, standard cells, and hard macros.

“The increase in DFM requirements at nanometer geometries has placed a significant strain on RF, analog and mixed-signal IC designers,” said Eric Filseth, president and CEO of Ciranova®. “By establishing an advanced and open reference flow that integrates robust automated layout technology, TSMC is helping their mixed-signal SoC customers bring differentiated silicon products to market more quickly.”

About Ciranova

Ciranova is electronic design automation (EDA) company focused on large productivity improvements in RF, analog and mixed-signal IC physical design. Complementary to existing design flows, Ciranova technology dramatically reduces the time and effort needed to develop device-level layout at both the circuit and PDK levels. Ciranova is a founding member of the Interoperable PDK Libraries (IPL) Alliance and supports the Si2 OpenAccess database. For more information please visit <http://www.ciranova.com>.

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