

CIRANOVA

# Helix

*Automated Analog Layout on OpenAccess – a Practical Approach*

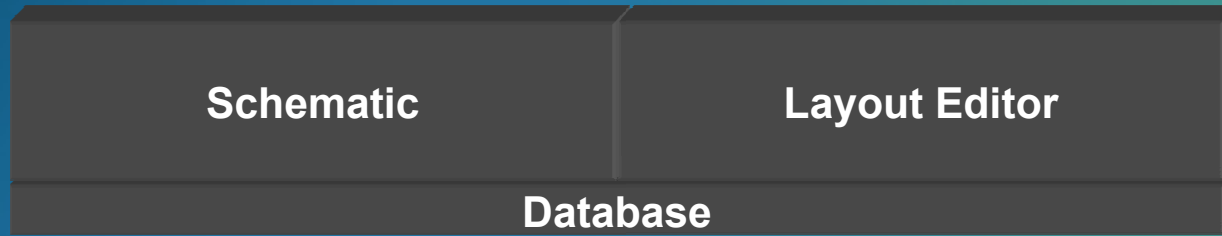
# THEN



1989

“Simple” design rules

Life cycle >> design time



Major widely-adopted analog IC layout EDA innovations

- Schematic-driven layout
- Extension languages (Skill ...)
- PCells
- Parasitic resimulation flow
- Shape-based routing (top level)

Plus: GUI and database work

# NOW



2009

DRC deck = 40K lines

Life cycle ~ design time

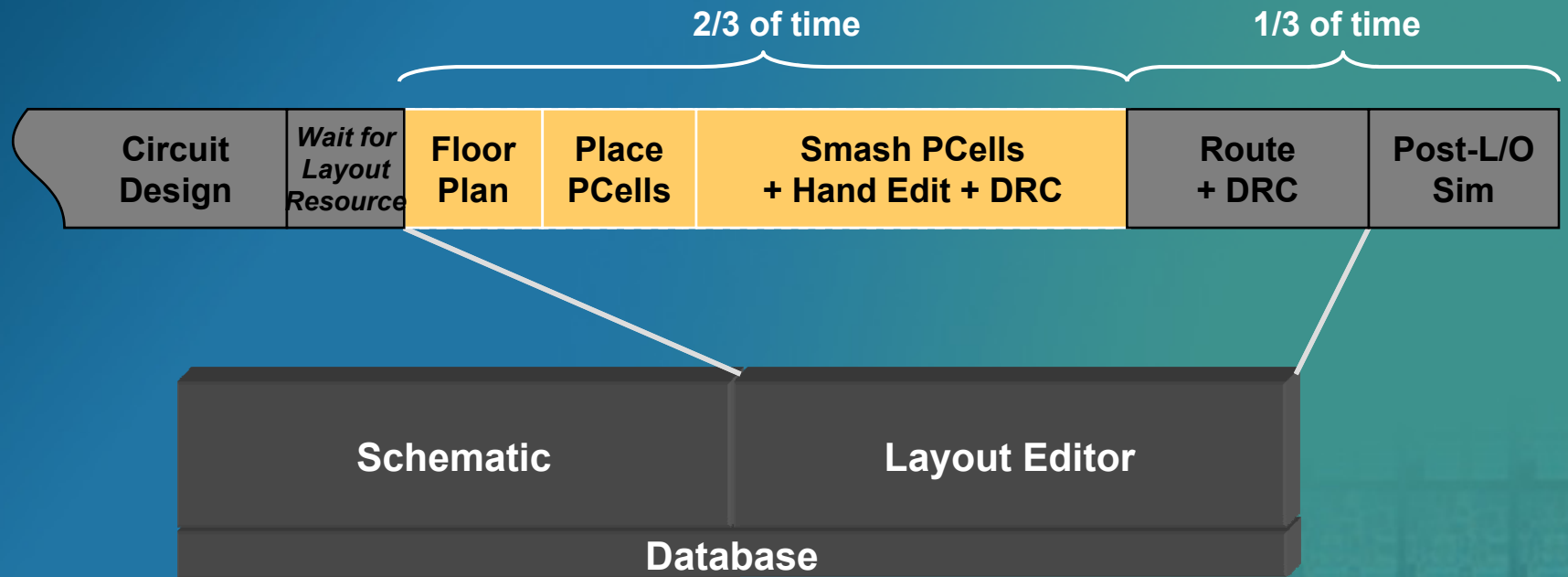
**“At 40nm, 70-80% of our design cycle will be in layout.”**

**- Director engineering, top 10 semi vendor**

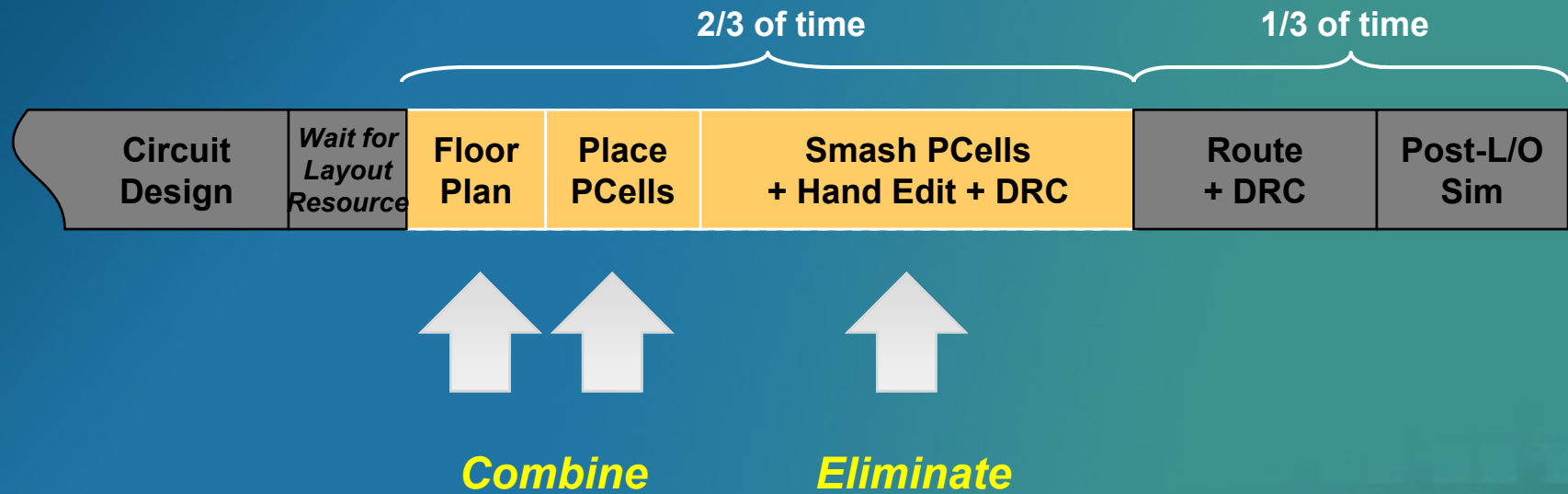
**“At 40nm, we click the interactive DRC for every device”**

**- Analog layout manager, top 10 semi vendor**

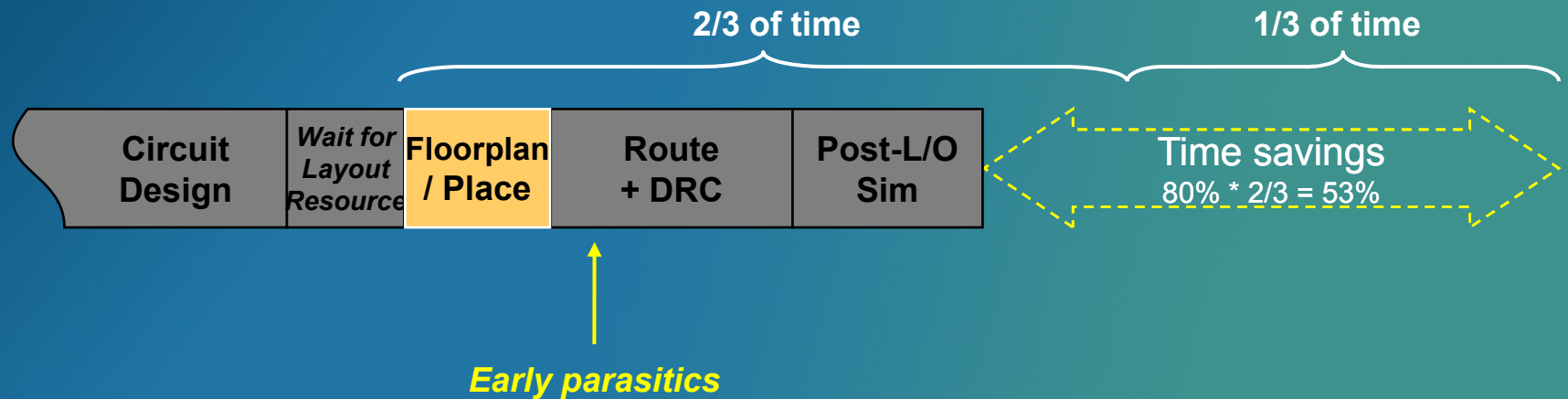
# How Analog Layout Works Today



# Placement Automation Can Cut 1/2



# Placement Automation Can Cut 1/2



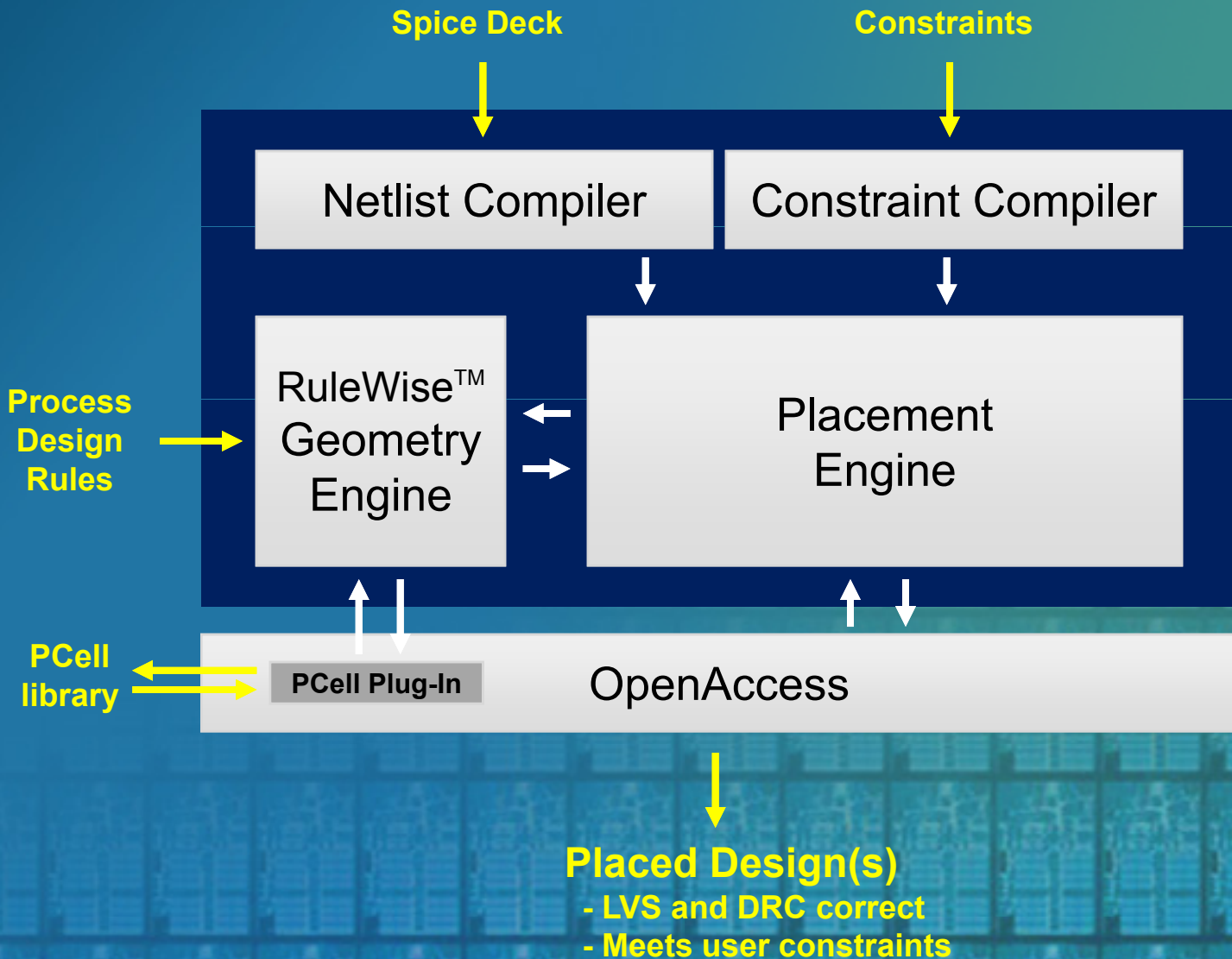
- **Completely automated**
  - Analog circuit requirements – matching, symmetry ...
  - Device-level – interdigitation, abutment, DRC-correct ...
- **Full device-level placement of the entire AMS block**
- **Easy to use and very little setup effort**

# Helix Analog Placement – Examples

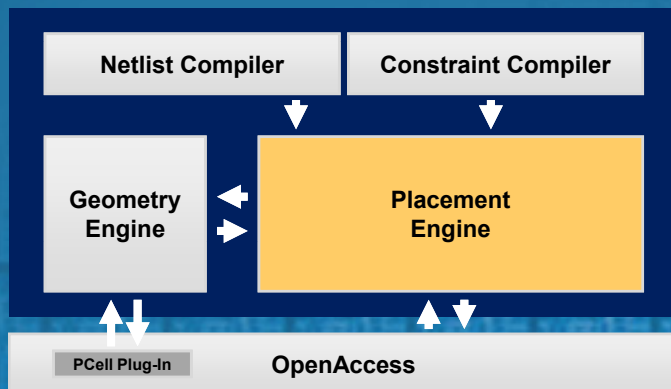
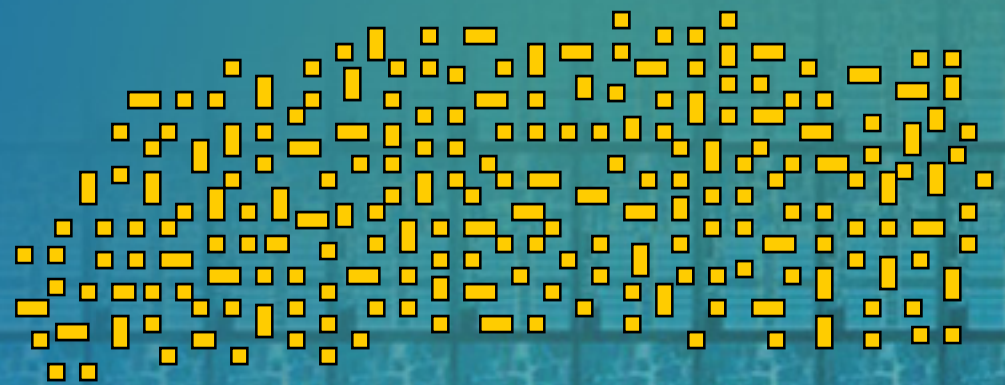
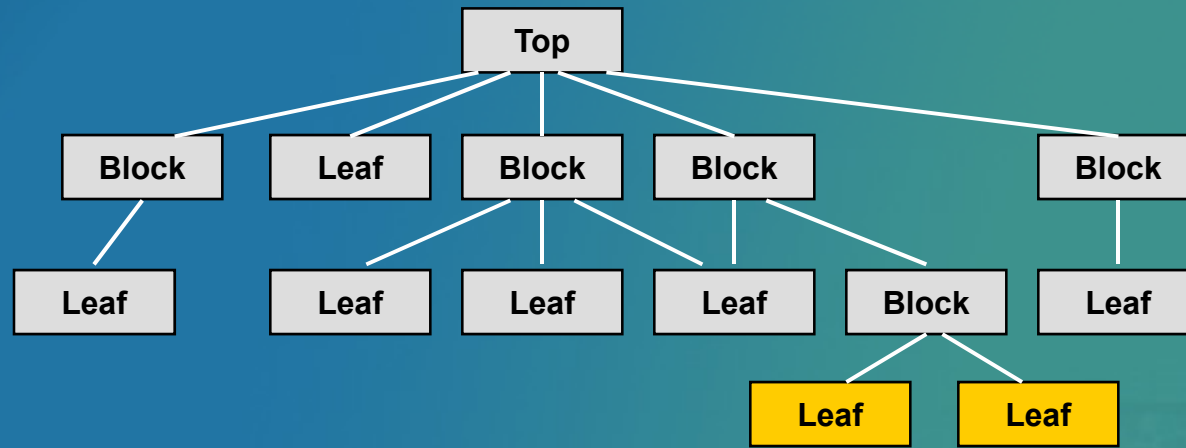
<u>Circuit</u>	<u>Total Time – Netlist to Final Placement *</u>
PLL, 1975 devices, 65nm	4.5 days
I/O slice, 1000 devices, 65nm	4 days
A/D block, 800 devices, 130nm	4 days
Squelch circuit, 200 devices, 65nm	1 day
Comparator, 40 devices, 65nm	½ day

\* *includes: consultation/review with circuit designer, all constraint development, all placement runs, final DRC*

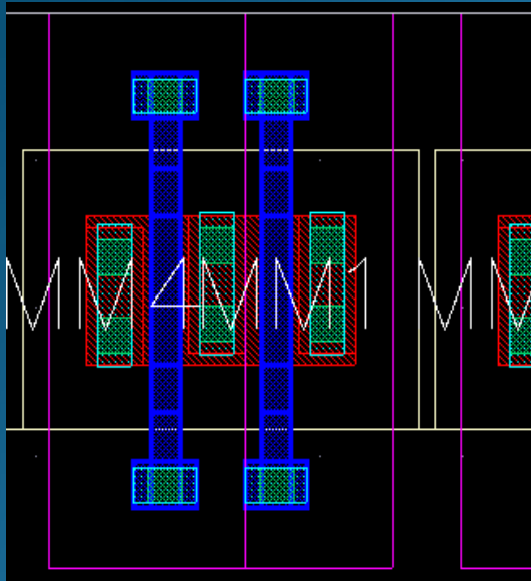
# Helix Architecture



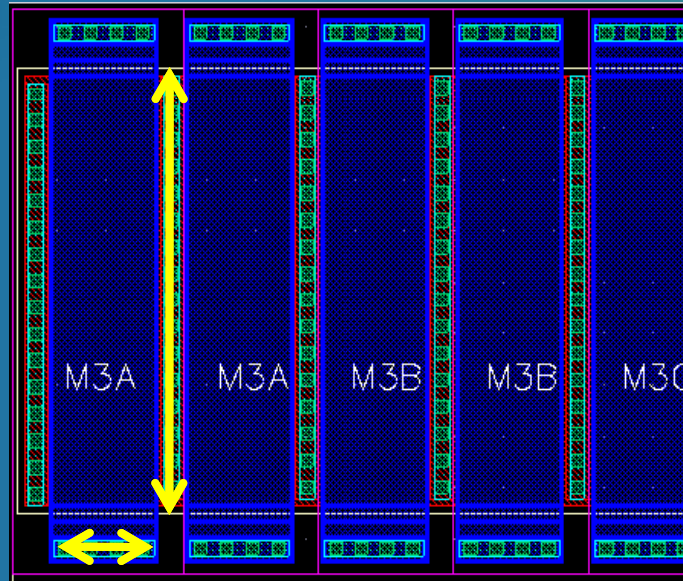
# Helix Architecture – Placement



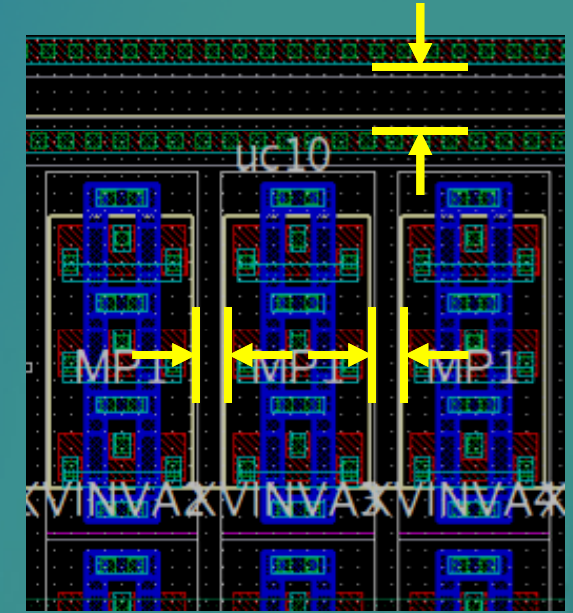
# Helix Architecture – Geometry



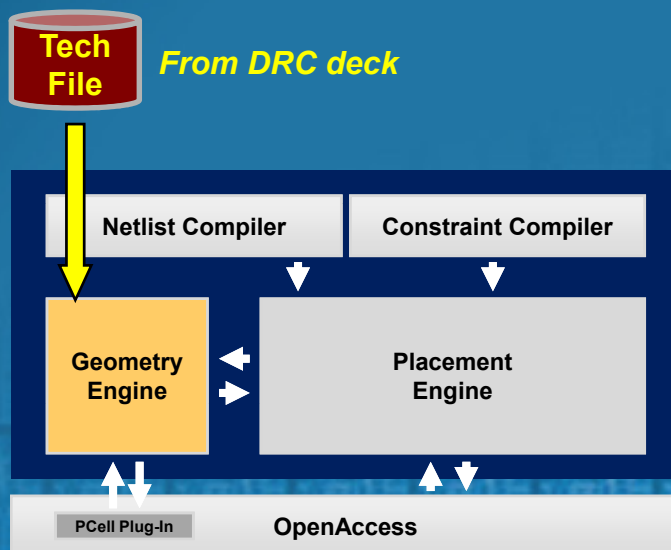
Abutment & well merging



Interdigitation

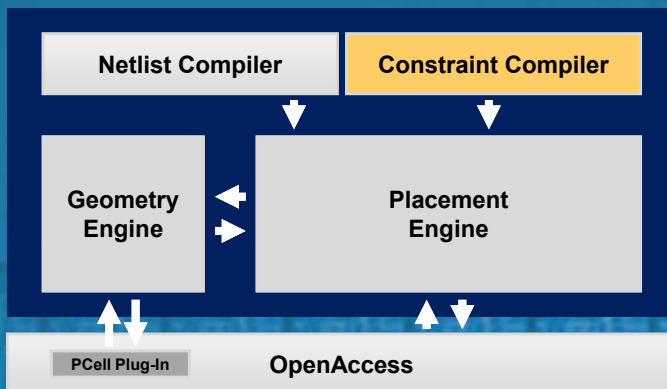
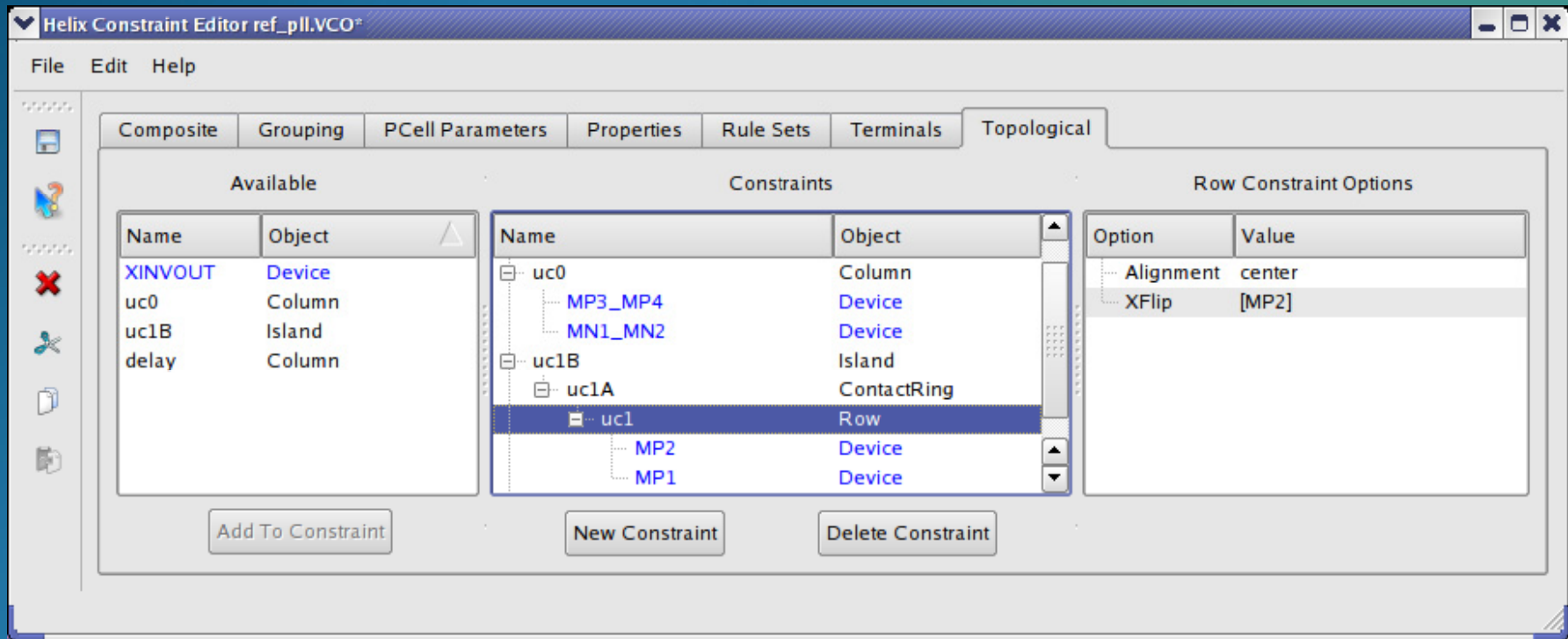


Device spacing



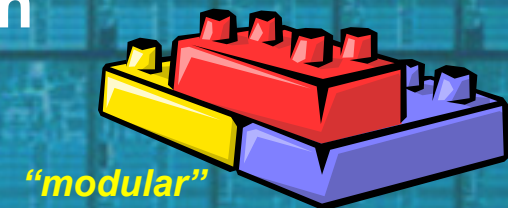
# Helix Architecture – Constraints

*Easy to use + no process-specific data needed*

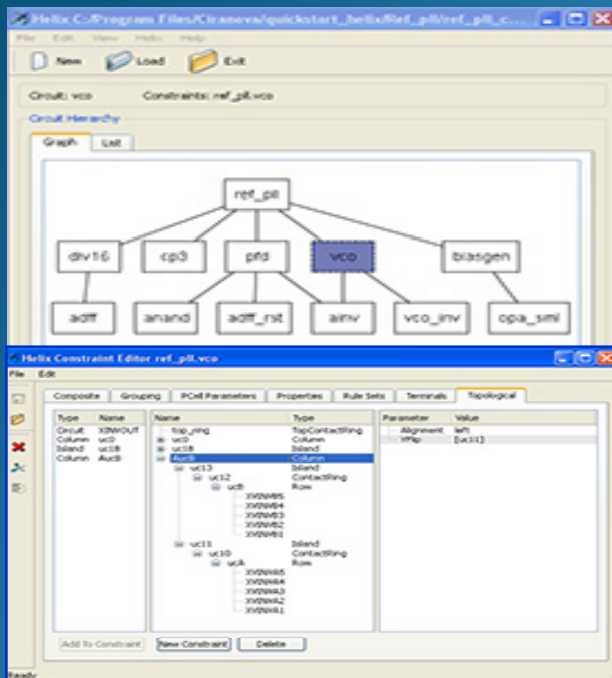


Column  
Row  
Mirror  
Group  
Guard ring  
Pattern

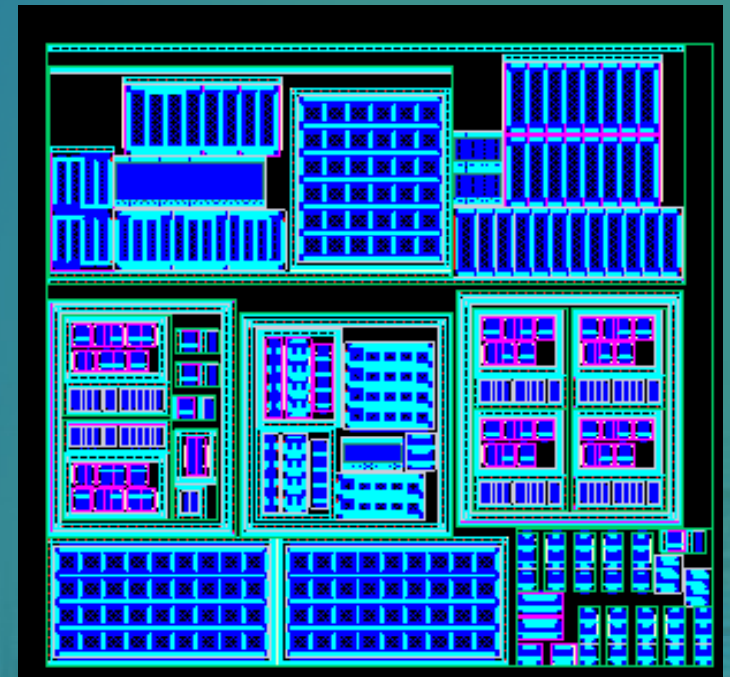
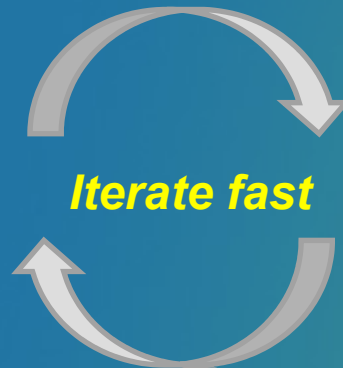
...



# Basic Helix Use Model – Iterate



Constraint Environment  
*Easy to Use*



Floorplan / placement  
*Very fast, always DRC-clean*

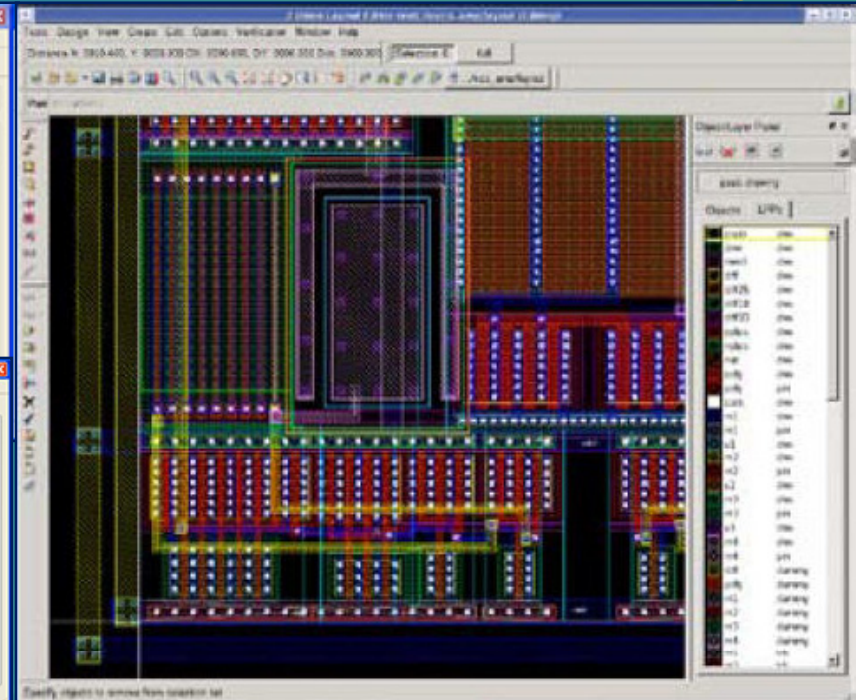
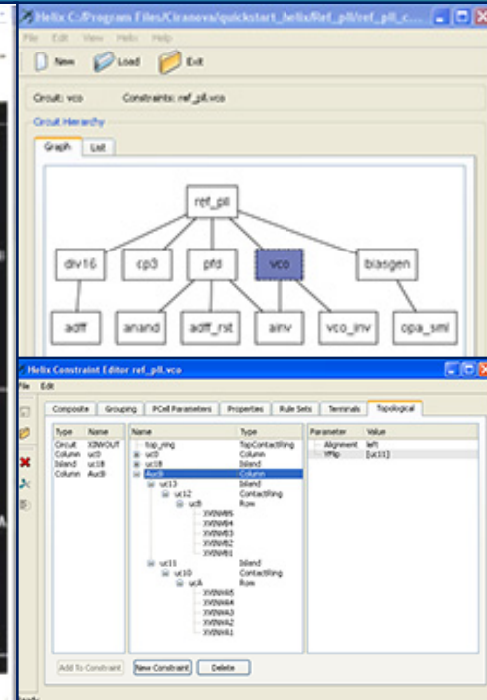
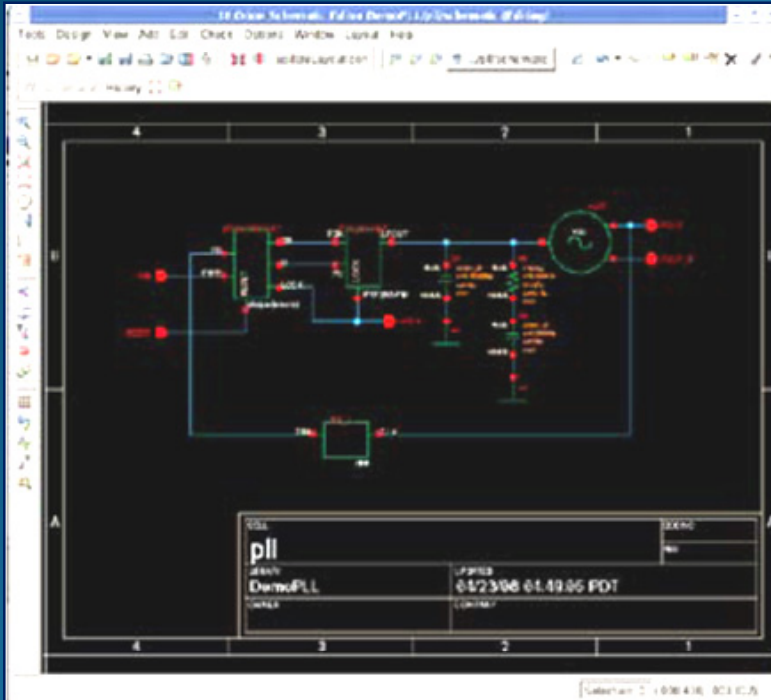
1. Run initial placement with minimal constraints or none at all
2. Add/adjust constraints and re-run placement – typical run times in minutes
3. Repeat #2 until all designer goals for placement met (final placement)

# OA-Based Analog/MS Design System

Capture

Helix Floorplan / Place

Route / Extract / Chip Finishing



OpenAccess

Interoperable PDK

Design Rules  
(65nm)

Design Rules  
(40nm)

Design Rules  
(32nm)

# Design Flow

The image shows a screenshot of the Orion Schematic Editor interface. The main window title is "1 Orion Schematic Editor myLib/ref\_pll/schematic (Editing)". The menu bar includes "Tools", "Design", "View", "Add", "Edit", "Check", "Options", "Window", "Ciranova", and "Help". The toolbar contains various icons for file operations, editing, and simulation. The main workspace displays a schematic diagram of a PLL (Phase-Locked Loop) circuit. The circuit includes several blocks: "BIASGEN" (with inputs VBG and VREF, and outputs IREFP1, IREFP2, IREFN1, IREFN2), "PFD" (with inputs CLRIN, REFCLK, FBCLK, and outputs UP, UPN, DOWN, DOWNN), "CP3" (with inputs UPN, IUP, IDOWN, DOWN), "BI16" (with inputs CLROUT and CLRIN), and two "MFLTCAP" blocks connected to a node labeled "055". The "Launch Helix Placer" dialog box is open in the foreground, showing the following configuration:

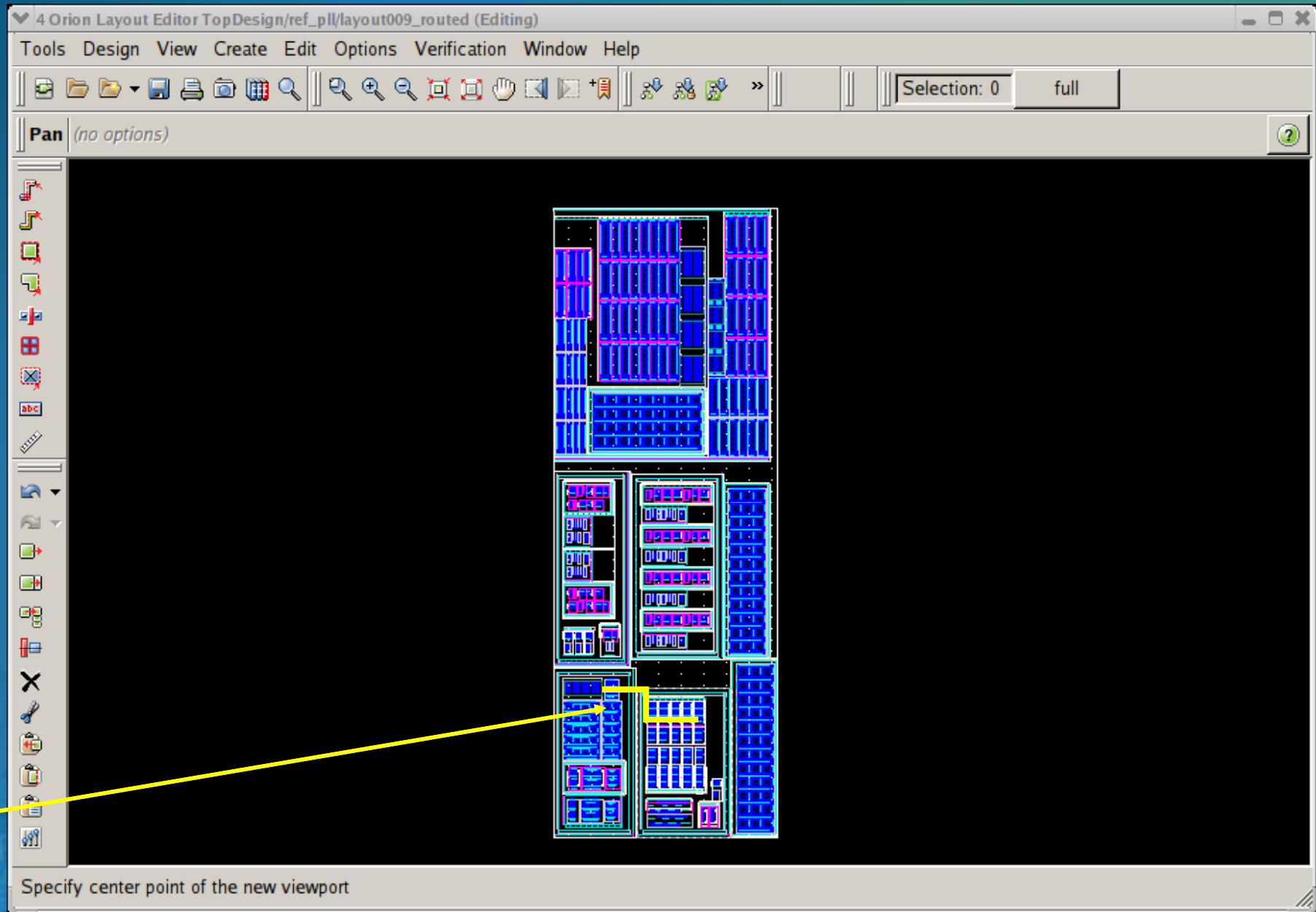
- Top Schematic: (empty)
- Library: myLib
- Cell: ref\_pll
- View: schematic
- Options:
  - Config: mo/header\_template.hxcfg
  - Constraints: demo/dist\_trkhold\_cr2.hxcsc
  - Device Map: per/helix/demo/device.map
  - Execute:  Foreground  Background

Buttons for "OK", "Apply", and "Cancel" are visible at the bottom of the dialog. The status bar at the bottom right shows "Selection: 0 ( 010.250, 002.062)".



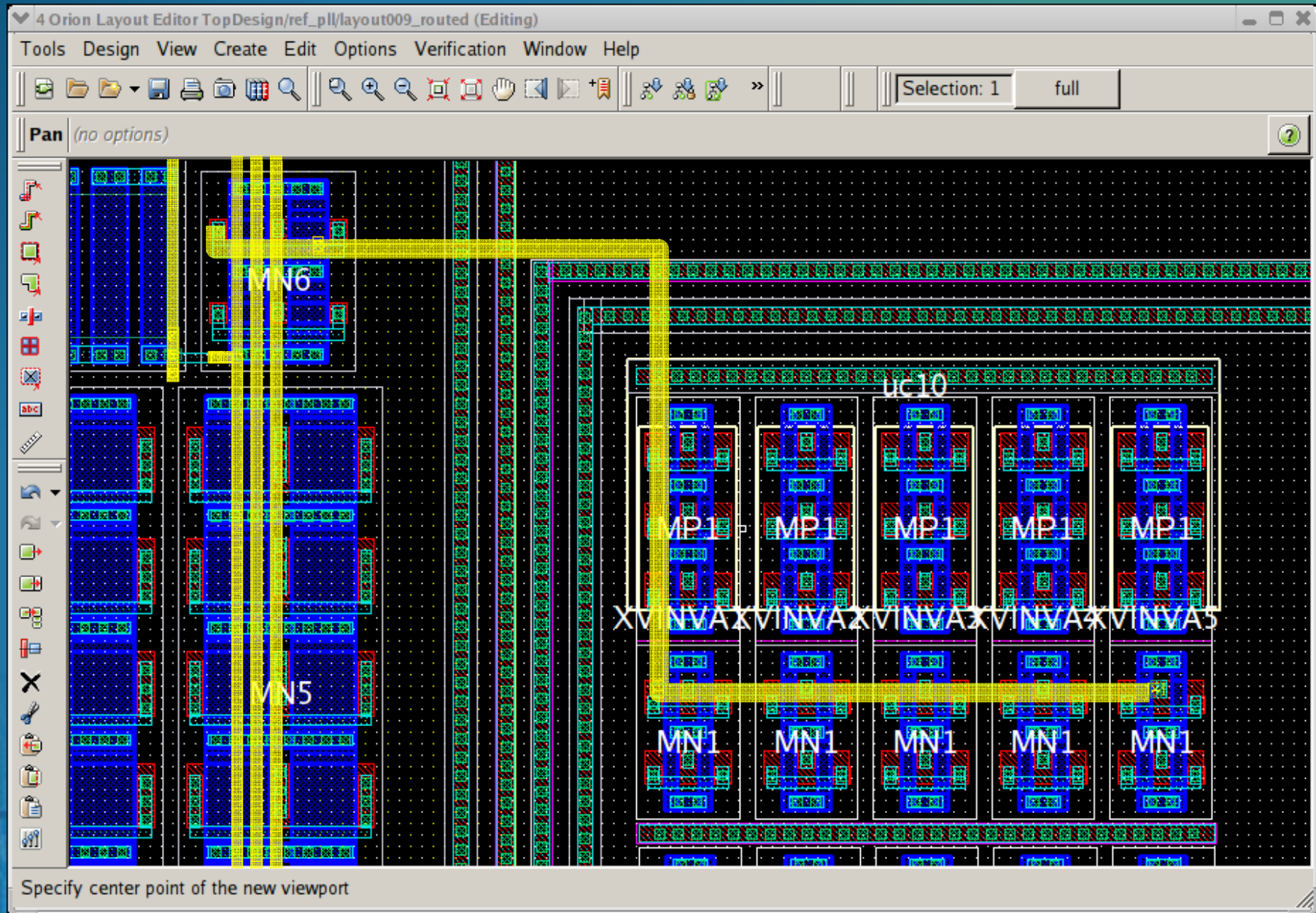
# Design Flow

*Choose this layout*



*Critical net*

# Design Flow



# Example Design

Block from a serdes, 65nm  
850 unmerged objects

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- Placement: 1 day
- Route + extract: 2.5 days

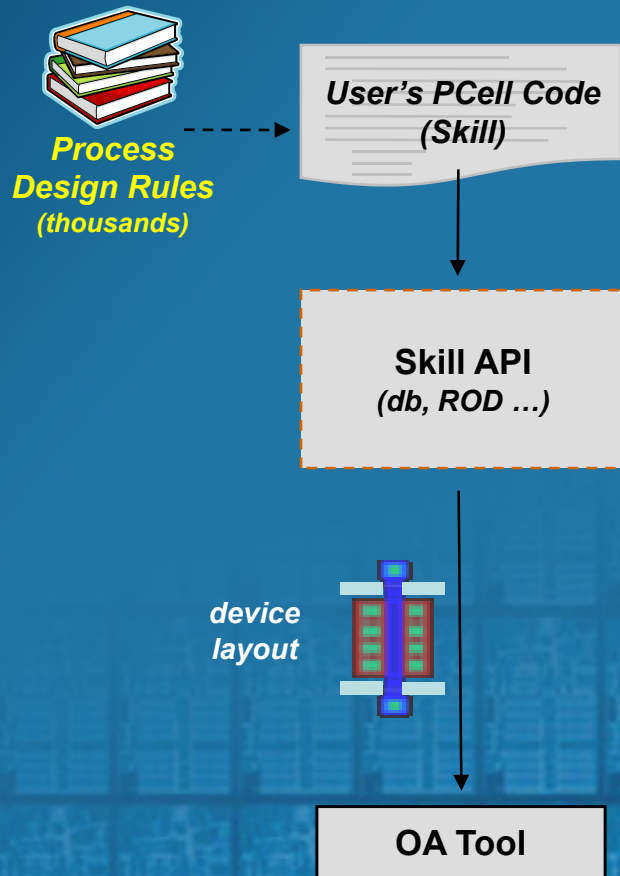
*New objective – reduce capacitance on xyz net*

- Re-place: ½ day
- Re-route + extract: 1.5 days

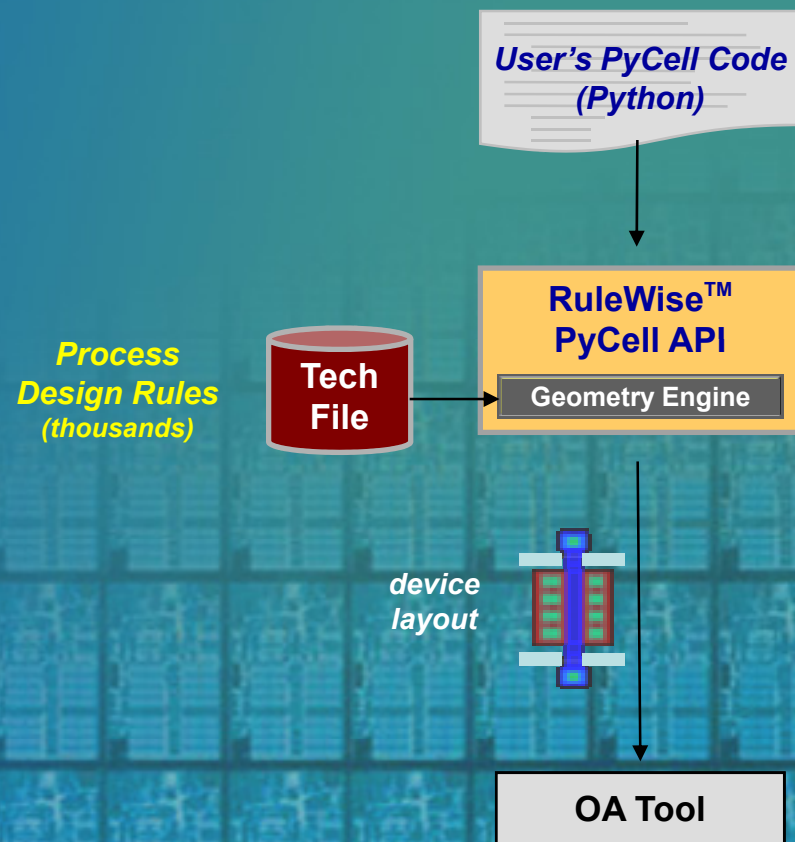


# Creating Process-Portable PCells

## Traditional PCells

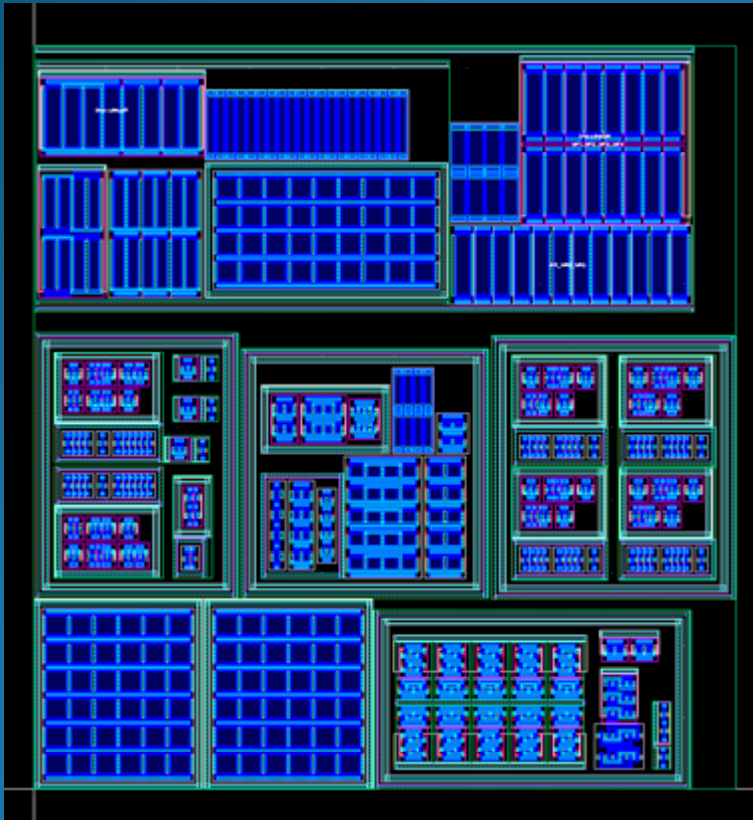


## PyCells

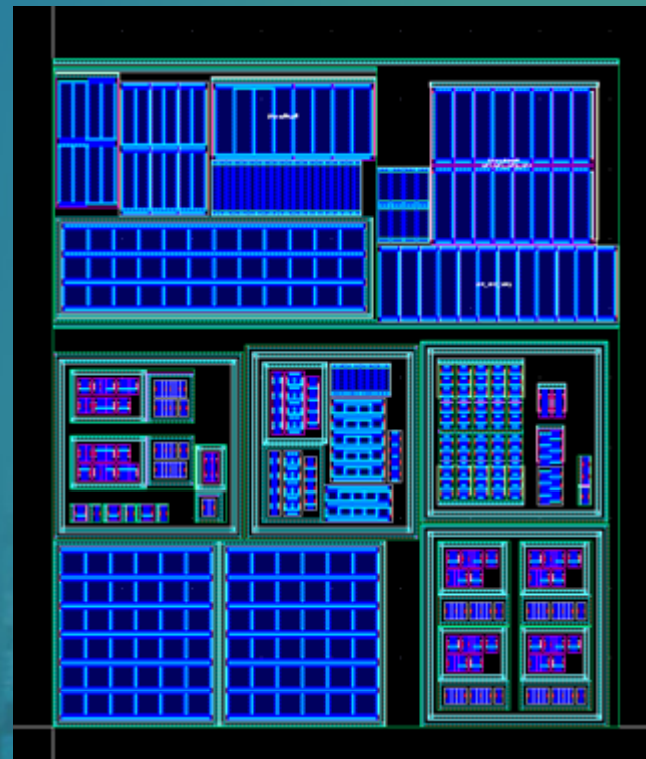


# Regenerate Layout on New Tech

90nm

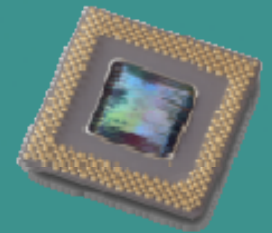
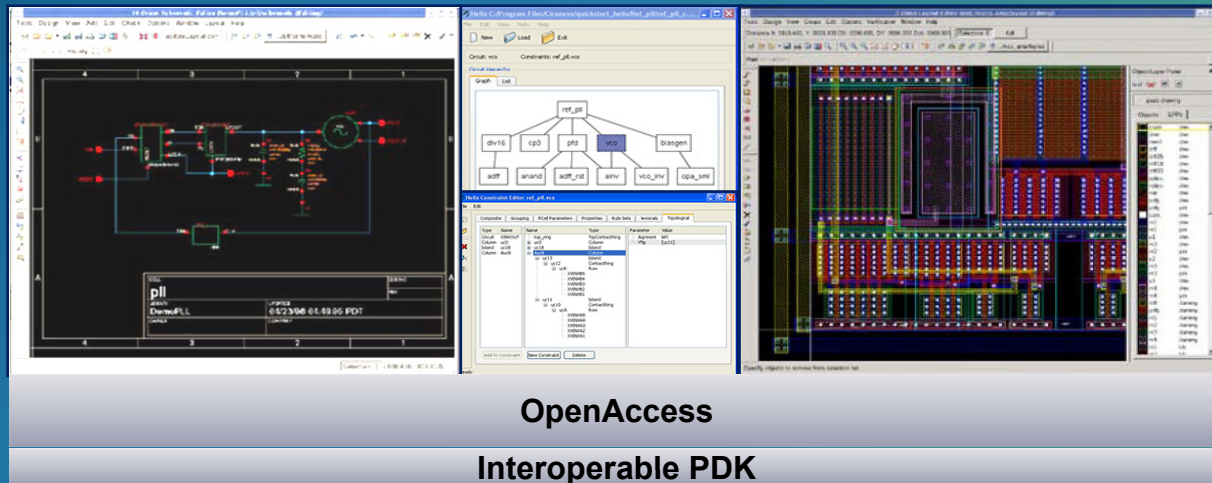


65nm



- Same constraints
- Same netlist (active devices resized)
- 65nm tech file
- Same PyCells w/ 65nm tech file

# New Analog Flow vs Traditional



- **Very significant differentiation today**
  - Cut analog layout cycle in half
  - Early parasitic analysis
  - Analog IP re-use support
- **More differentiation tomorrow**
  - Architecture for ultra-complex process and DFM rules
  - Automatic routing even higher productivity